



Australian Government

UEEEEC0054 Provide gate array solutions for complex electronics systems

Release: 1

UEEEEC0054 Provide gate array solutions for complex electronics systems

Modification History

Release 1. This is the first release of this unit of competency in the UEE Electrotechnology Training Package.

Application

This unit involves the skills and knowledge required to design and develop electronic systems using gate array technology.

It includes working safely, following gate array design brief and interpreting device specifications, using appropriate development software, testing operation and verifying compliance of the of the design against the final brief, and documenting design and development work.

No licensing, legislative or certification requirements apply to this unit at the time of publication.

Pre-requisite Unit

UEECD0007 Apply work health and safety regulations, codes and practices in the workplace

Competency Field

Electronics and Communications

Unit Sector

Electrotechnology

Elements and Performance Criteria

ELEMENTS

Elements describe the essential outcomes.

1 Prepare to design gate array system

PERFORMANCE CRITERIA

Performance criteria describe the performance needed to demonstrate achievement of the element.

1.1 Work health and safety (WHS)/occupational health and safety (OHS) requirements and workplace procedures for a given work area are identified and applied

- 1.2 Operational safety procedures for a given work area are obtained and understood
 - 1.3 Extent of the proposed gate array system design and circuit development is determined from design brief or in consultation with appropriate person/s
 - 1.4 Design and circuit development work is planned to meet scheduled timelines in consultation with others involved
 - 1.5 Materials and devices/components required for the design work are selected on compatibility of their specifications with system requirements and project budget constraints
 - 1.6 Tools, equipment, software and testing devices needed to carry out the work are obtained and checked for correct operation and safety
- 2 Design and develop circuit gate array system**
 - 2.1 WHS/OHS risk control measures and workplace procedures for carrying out the design work are followed
 - 2.2 Gate array system and industry compliance standards are applied to the design
 - 2.3 Alternative arrangements for the design and circuit development are considered in accordance with the requirements outlined in the design brief
 - 2.4 Safety, functional and budget considerations are incorporated in the design
 - 2.5 Circuit device and circuits are constructed and tested for compliance with the design brief and regulatory requirements
 - 2.6 Circuit malfunctions are rectified and retested to ensure effective operation with the design
 - 2.7 Gate array system design and development is documented for submission to appropriate person/s for approval
 - 2.8 Solutions to unplanned situations are provided in accordance with workplace policies
- 3 Obtain approval for design and circuit**
 - 3.1 Gate array system design is presented and explained to client representative and/or relevant person/s

development of gate array system and documentation

- 3.2** Requests for design modifications are negotiated with relevant person/s within the constraints of workplace policies
- 3.3** Final design and circuit development are documented and approval obtained from appropriate person/s
- 3.4** Quality of work is monitored against design brief, performance agreement and/or workplace procedures or industry standards

Foundation Skills

Foundation skills essential to performance are explicit in the performance criteria of this unit of competency.

Range of Conditions

Range is restricted to essential operating conditions and any other variables essential to the work environment.

Non-essential conditions may be found in the UEE Electrotechnology Training Package Companion Volume Implementation Guide.

Designing and developing a gate array system must include at least the following:

- three input/output (I/O) devices or functions

Unit Mapping Information

This unit replaces and is equivalent to UEENEEH189A Provide Gate Array solutions for complex electronics systems.

Links

Companion Volume implementation guides are found in VETNet - - <https://vetnet.gov.au/Pages/TrainingDocs.aspx?q=b8a8f136-5421-4ce1-92e0-2b50341431b6>

Assessment Requirements for UEEEC0054 Provide gate array solutions for complex electronics systems

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Performance Evidence

Evidence required to demonstrate competence in this unit must be relevant to and satisfy all of the requirements of the elements, performance criteria and range of conditions on at least two separate occasions and include:

- constructing, inspecting and testing circuit gate array device and circuits in accordance with design brief and regulatory requirements
- dealing with unplanned situations in accordance with workplace procedures in a manner that minimises risk to personnel and equipment
- designing gate array system in accordance with workplace procedures
- developing outlines of alternative designs and comparing advantages and disadvantages on each
- developing the gate array design within the safety and functional requirements and budget limitations
- documenting and presenting design effectively
- implementing relevant work health and safety (WHS)/occupational health and safety (OHS) requirements, including the use of risk control measures
- negotiating design alteration requests and obtaining approval for final gate array design system
- verifying compliance of the design against the final brief.

Knowledge Evidence

Evidence required to demonstrate competence in this unit must be relevant to and satisfy all of the requirements of the elements, performance criteria and range of conditions and include knowledge of:

- gate array fundamentals
- hardware design language
- programmable logic device (PLD), including:
 - types of PLDs
 - features of complex programmable logic device (CPLD) devices
 - features of field programmable gate array (FPGA) devices
 - input/output (I/O) logic family assignment for FPGA

- relevant job safety assessments or risk mitigation processes
- relevant WHS/OHS legislated requirements
- relevant workplace documentation
- relevant workplace policies and procedures.

Assessment Conditions

Assessors must hold credentials specified within the Standards for Registered Training Organisations current at the time of assessment.

Assessment must satisfy the Principles of Assessment and Rules of Evidence and all regulatory requirements included within the Standards for Registered Training Organisations current at the time of assessment.

Assessment must occur in suitable workplace operational situations where it is appropriate to do so; where this is not appropriate, assessment must occur in simulated suitable workplace operational situations that replicate workplace conditions.

Assessment processes and techniques must be appropriate to the language, literacy and numeracy requirements of the work being performed and the needs of the candidate.

Resources for assessment must include access to:

- a range of relevant exercises, case studies and/or simulations
- relevant and appropriate materials, tools, equipment and personal protective equipment (PPE) currently used in industry
- resources that reflect current industry practices in relation to designing and developing gate array systems
- applicable documentation, including workplace procedures, equipment specifications, regulations, codes of practice and operation manuals.

Links

Companion Volume implementation guides are found in VETNet - -

<https://vetnet.gov.au/Pages/TrainingDocs.aspx?q=b8a8f136-5421-4ce1-92e0-2b50341431b6>